# On a eRHIC silicon detector:

# studies/ideas

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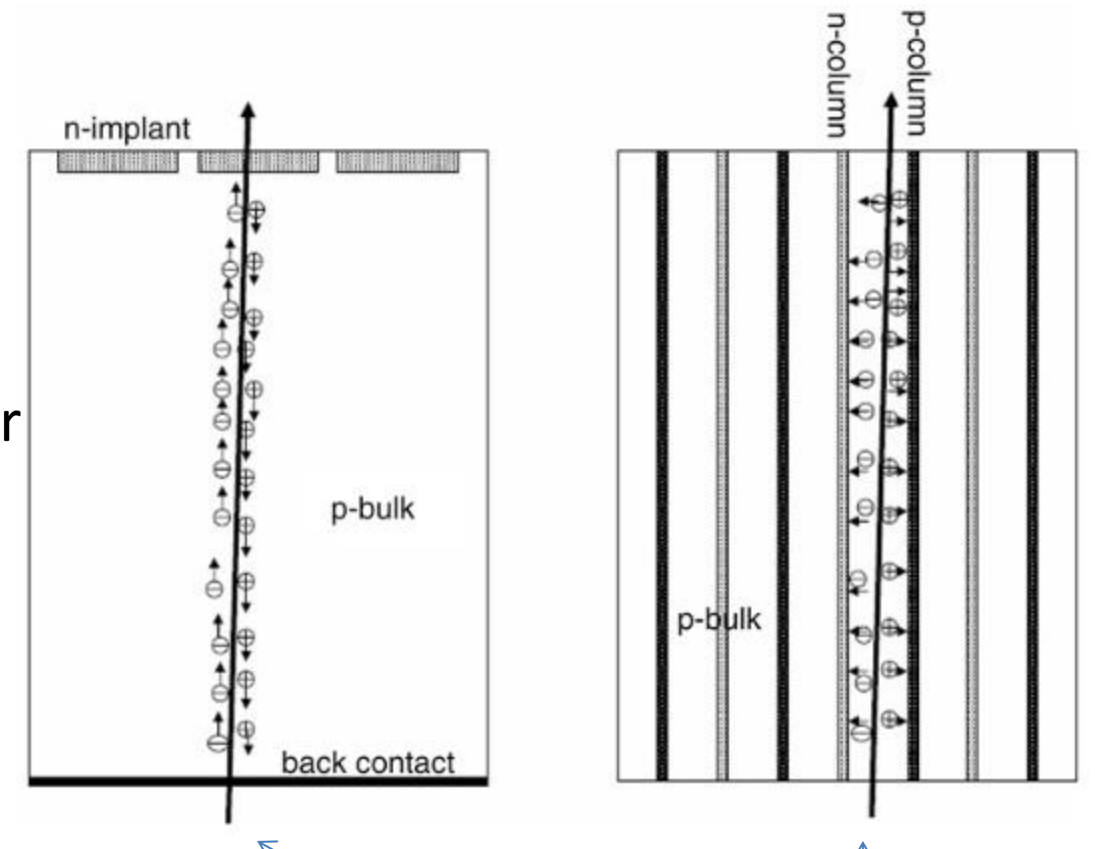
BNL EIC Task Force Meeting
May 16th 2013

# Summary

- Summary on silicon detectors
- Monolithic Pixel MIMOSA
- Tests ongoing
- Plans for the future

# Detection of a charged particle in a silicon detector

PLANAR sensor




3D Sensor

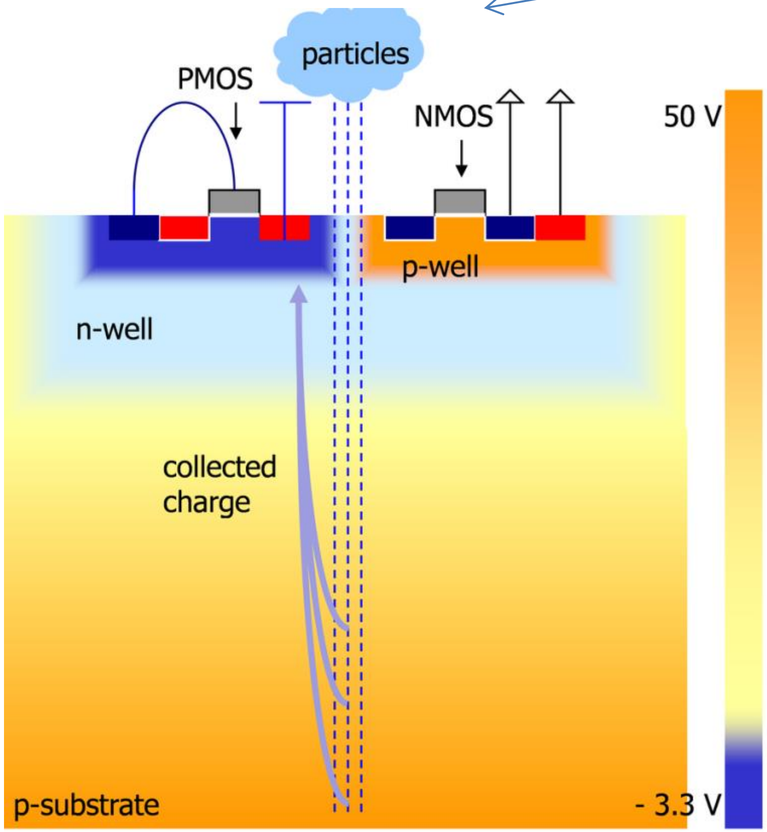
Ionizing particle

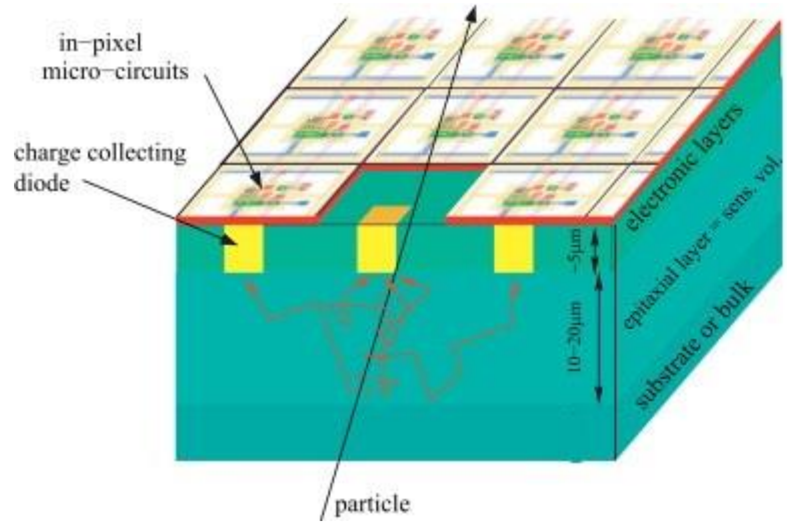
# Charge collection in a silicon detector

PLANAR biased sensor:
Electric Field charge collection

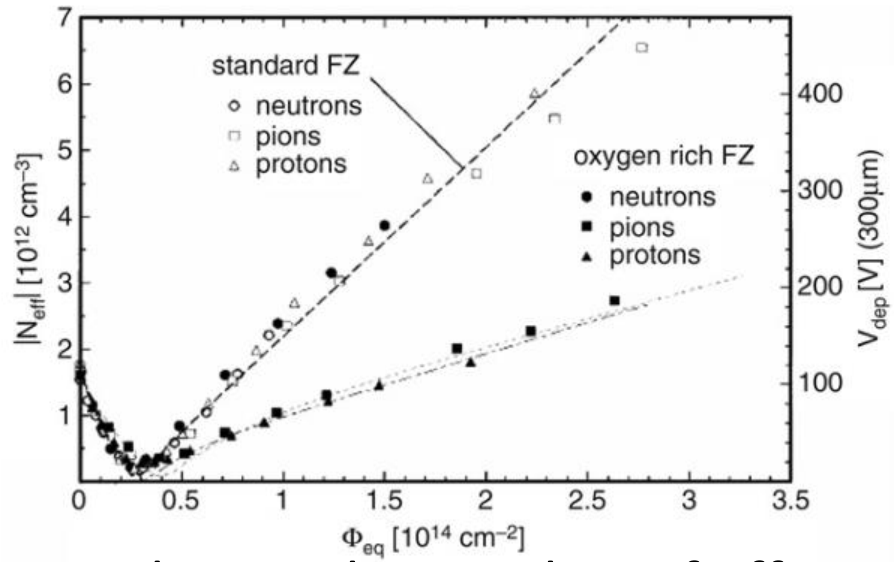
MAPS
Thermal charge collection

Ionizing particle



# Effect of aging on the depletion Voltage




The radiations change the number of effective charge carrier in the silicon.

- One result is that bias voltage required to keep fully depleted a sensor can increase a lot.
- Another effect is the increase of the noise.

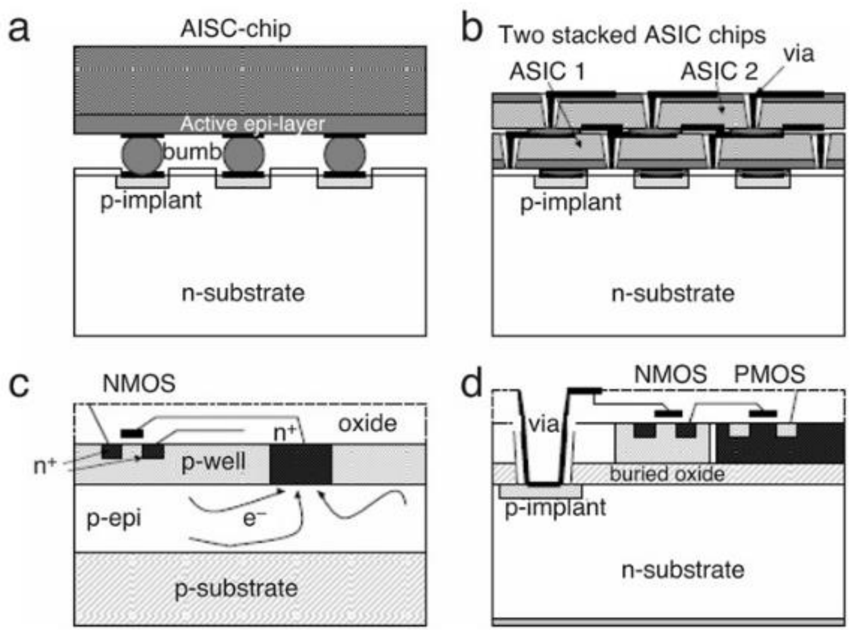
The *1 MeV equivalent neutron fluence* is the fluence of 1 MeV neutrons producing the same damage in a detector material as induced by an arbitrary particle fluence with a specific energy distribution.

# Silicon Pixel technologies

(the figures have different scale)

b=3D Integration:
Two stacked ASIC chips

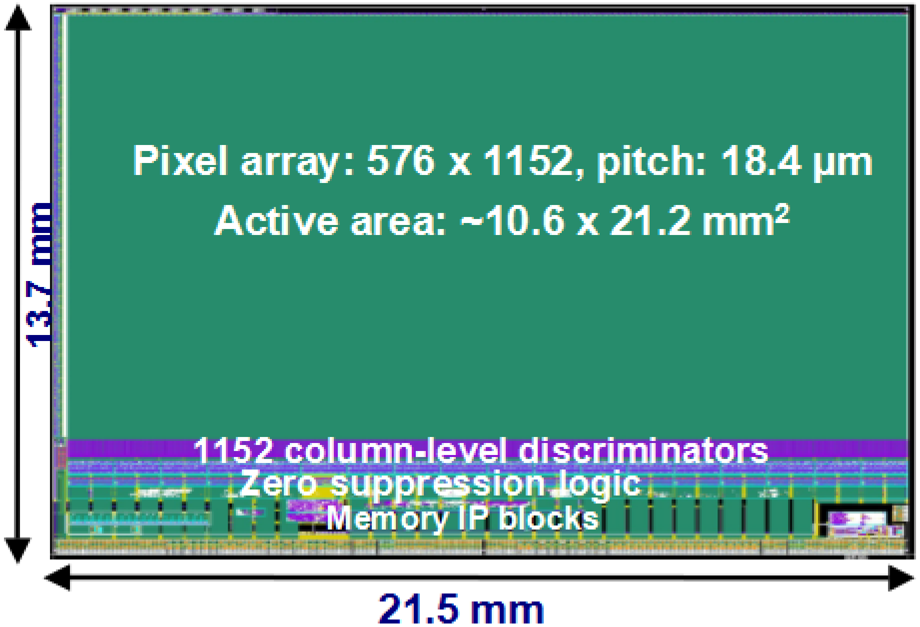
a=Hybrid




c=Monolithic (MAPS)

Silicon On Insulator (S.O.I)

# MIMOSA 26



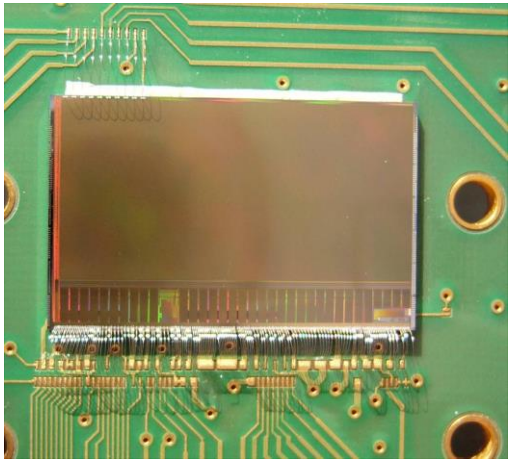

- active area ~2 $cm^2$
- 0.35 μm technology.
- binary output

(3.5 - 4 μm spatial resolution)

- in-pixel CDS + preamp.
- column level discrimination
- power dissipated ~280 $mW/cm^2$

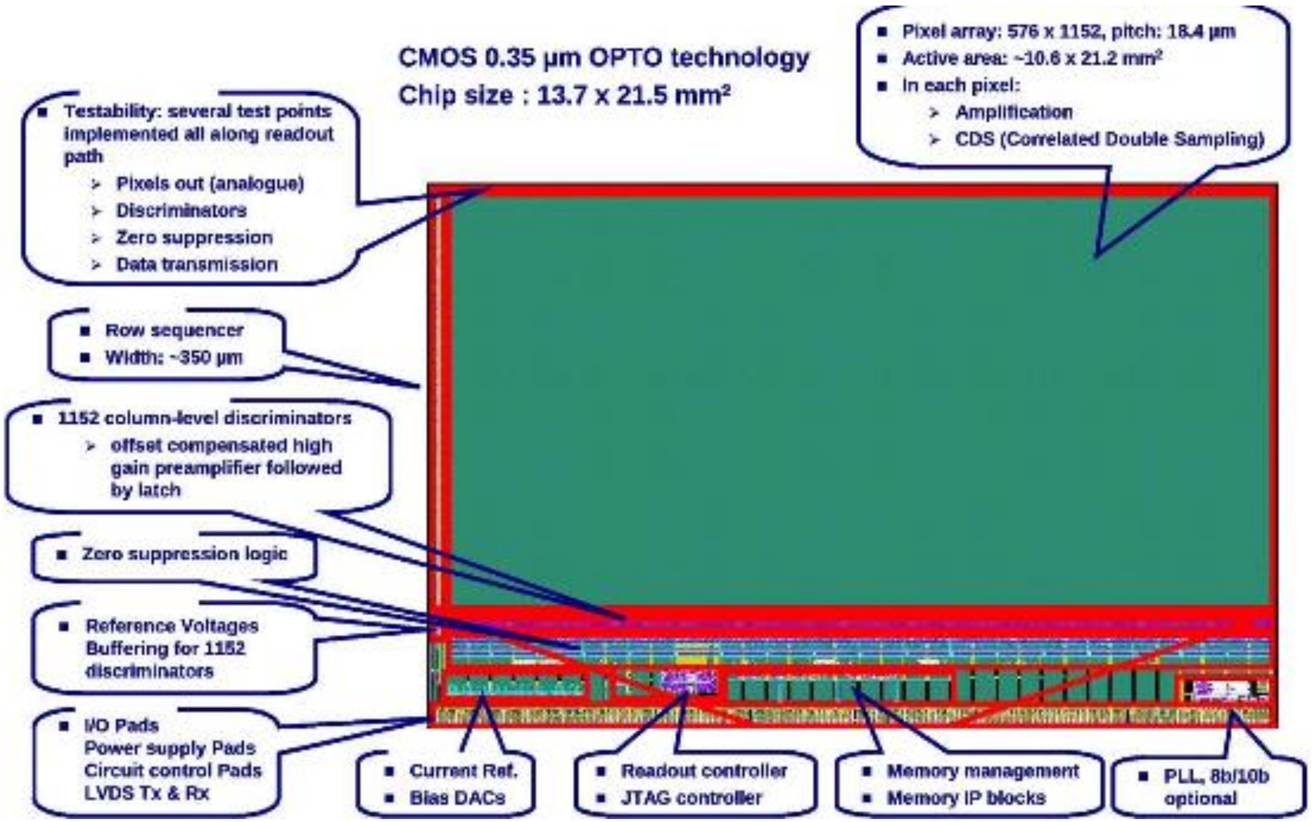
(rolling shutter)

- integration time ~100μs
- 120 μm thickness.



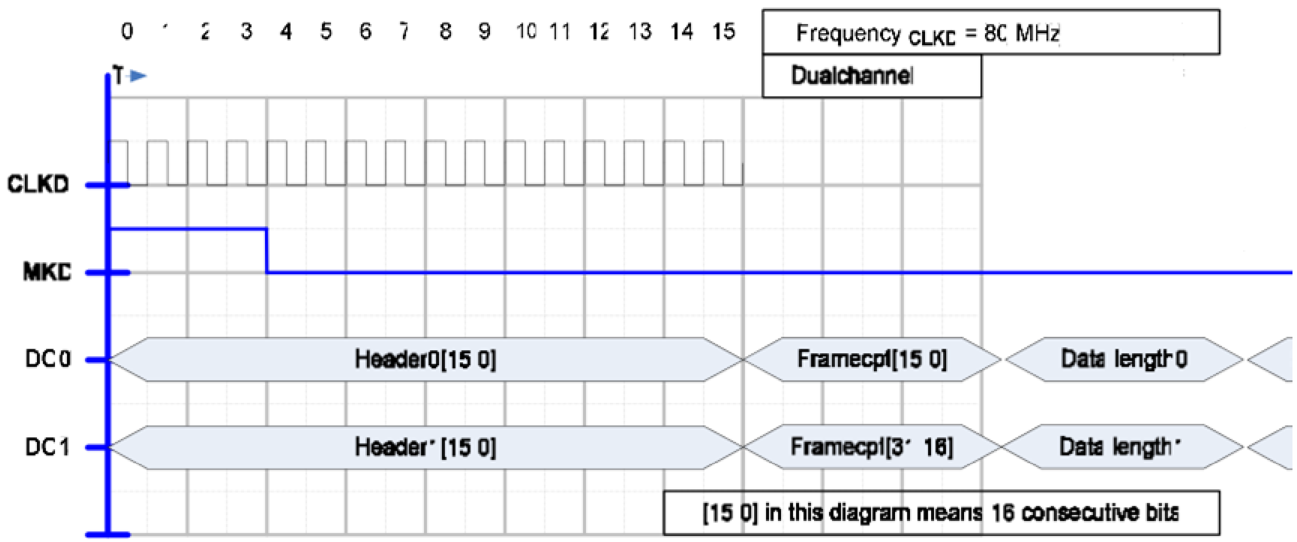
Test board implementation of a array

# MIMOSA 26



CMOS 0.35 µm OPTO technology
Chip size : 13.7 x 21.5 mm²
Pixel array: 576 x 1152, pitch: 18.4 µm
Active area: ~10.6 x 21.2 mm²
In each pixel:
Amplification
CDS (Correlated Double Sampling)
Testability: several test points implemented all along readout path
Pixels out (analogue)
Discriminators
Zero suppression
Data transmission
Row sequencer
Width: ~350 µm
1152 column-level discriminators
offset compensated high gain preamplifier followed by latch
Zero suppression logic
Reference Voltages Buffering for 1152 discriminators
I/O Pads
Power supply Pads
Circuit control Pads
LVDS Tx & Rx
Current Ref.
Bias DACs
Readout controller
JTAG controller
Memory management
Memory IP blocks
PLL, 8b/10b optional

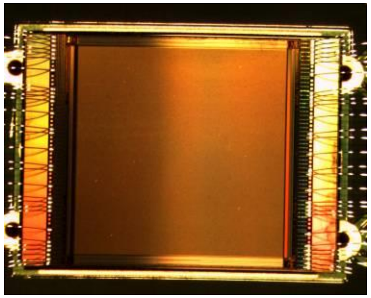
# MIMOSA 26: data output structure



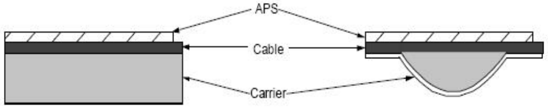

With the digital type chip the output are only the coordinates in the array (column and row)

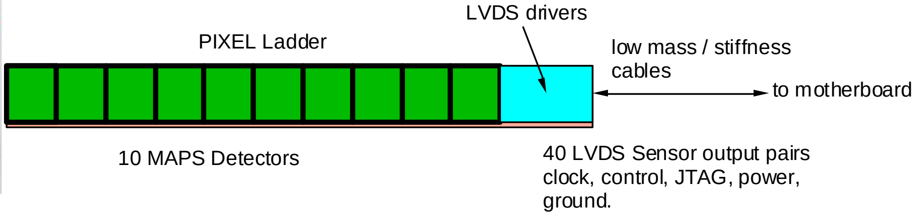
# From a chip to a ladder: STAR PXL

- ***Industrial thinning* of the support *(via STAR collaboration at LBNL)***
  - *~50 µm, expected to ~30-40 µm*
    - *Ex. MIMOSA18 (5.5×5.5 mm² thinned to 50 µm)*



- ***A ladder equipped with MIMOSA 28 chips (developed in LBNL)***
  - *STAR ladder (~< 0.3 % $X_0$ ) → ILC (<0.2 % $X_0$ )*

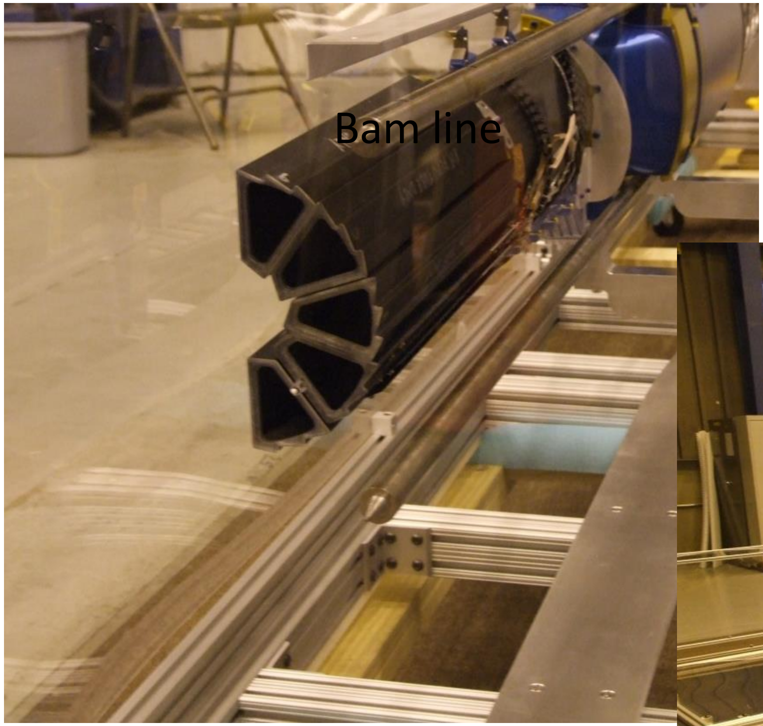



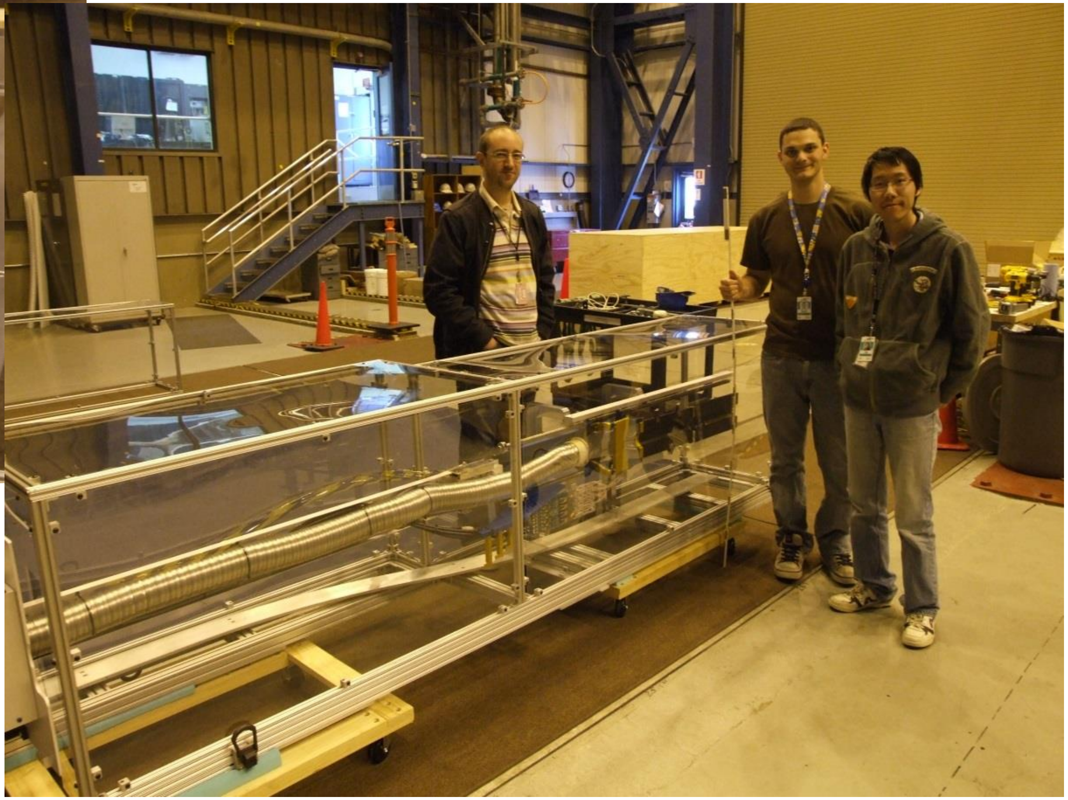




| | % radiation length |
|---|---|
| MIMOSA detector | 0.0534 |
| Adhesive | 0.0143 |
| Cable assembly | 0.090 |
| Adhesive | 0.0143 |
| CF / RVC carrier | 0.11 |
| Total | 0.282 |

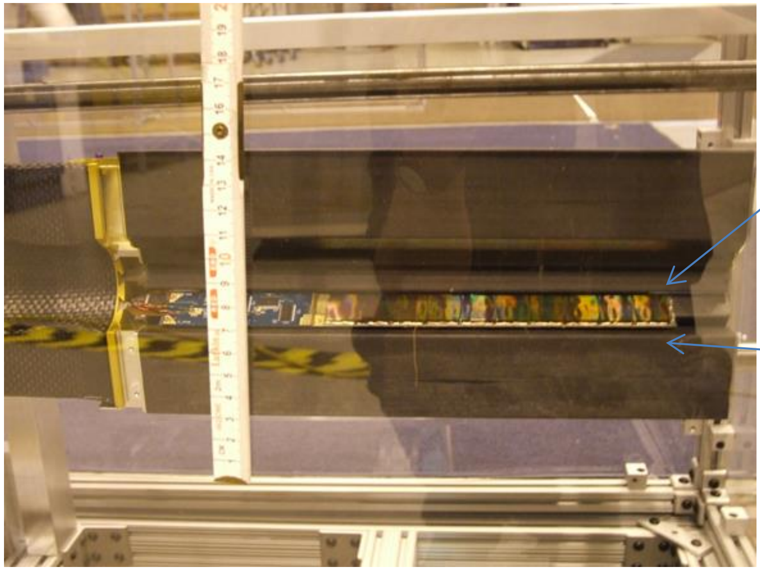
- ***Edgeless dicing / stitching → alleviate material budget of flex cable***

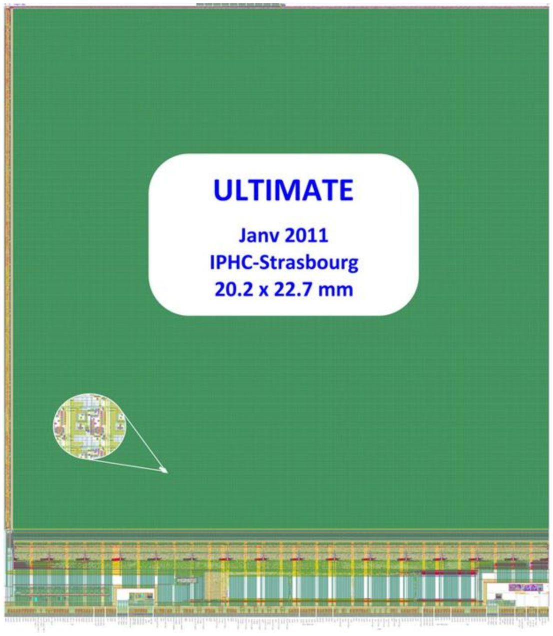
# Implementation in a real detector: STAR PXL



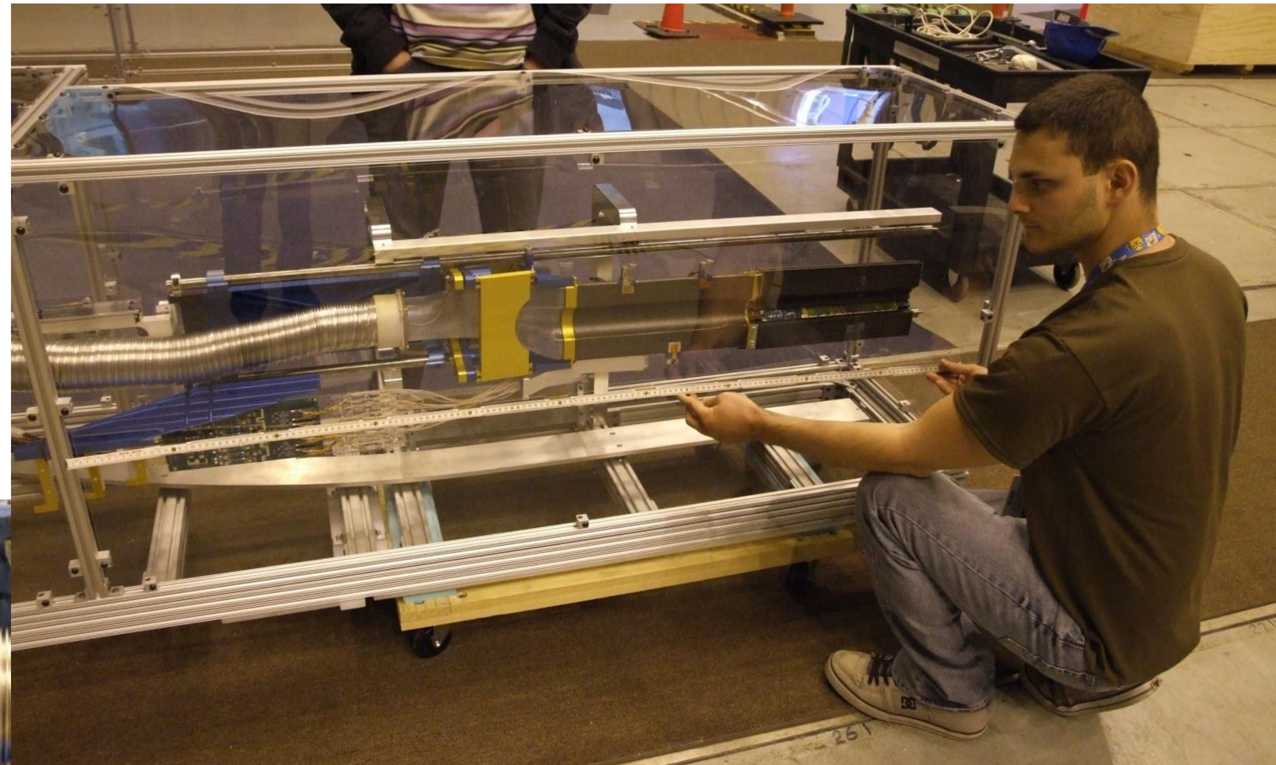



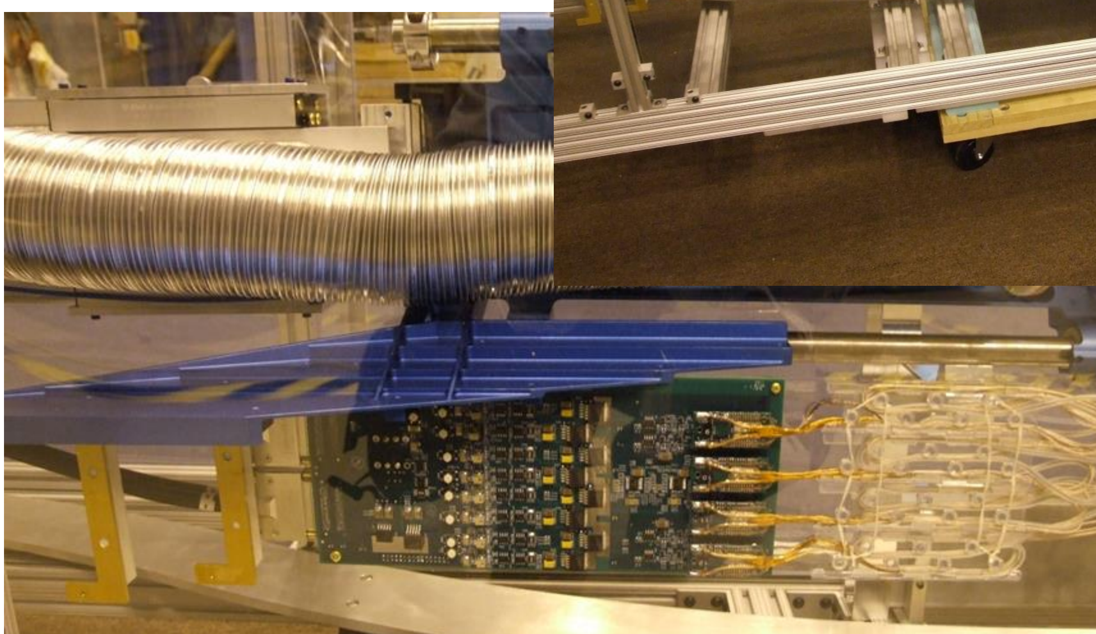
# STAR PXL






# STAR PXL





# Studies ongoing

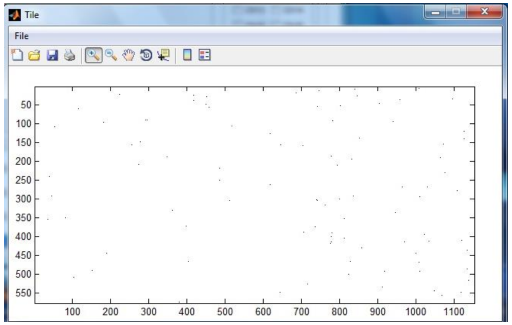
BNL setup:

- 1 Mimosa 26 array with digital output
- DAQ system

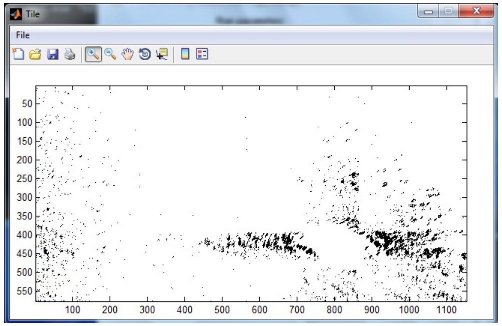
Equipment acquired:

- Manual and motorized stages (trans. +rot)
- 40 mW Laser + optic

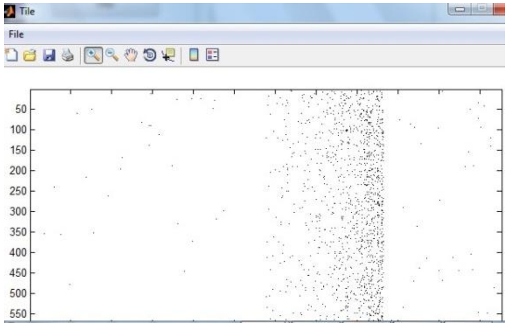
Noise




Scattered Laser Signal




Calibration



# Beam test at BNL NSRL

NSRL Beam line

Beams available

| Ion Species [1] | Energy [2] (MeV/nucleon) | Maximum Intensity [3] (ions per spill) |
|---|---|---|
| H-1 | 50 - 2500 | $6.4 \times 10^{11}$ |
| He-4 | 300 | $0.88 \times 10^{10}$ |
| C-12 | 135 - 1000 | $1.2 \times 10^{10}$ |
| O-16 | 100 - 1000 | $0.4 \times 10^{10}$ |
| Ne-20 | 300 | $0.10 \times 10^{10}$ |
| Si-28 | 94 - 1000 | $0.3 \times 10^{10}$ |

First Test on June $10^{th}$ with proton and carbon beam.

- Test the setup in a real beam condition.
- Study the charge sharing for Protons and Carbon Ions beam for a large incident angle . (between 45 and 90 degree).

Expected results with a digital Chip:

- Observe differences in signals collection and clustering between not perpendicular beams of protons and ions.
- Investigate limits of the DAQ structure.

# Studies to do with laser and analog chip

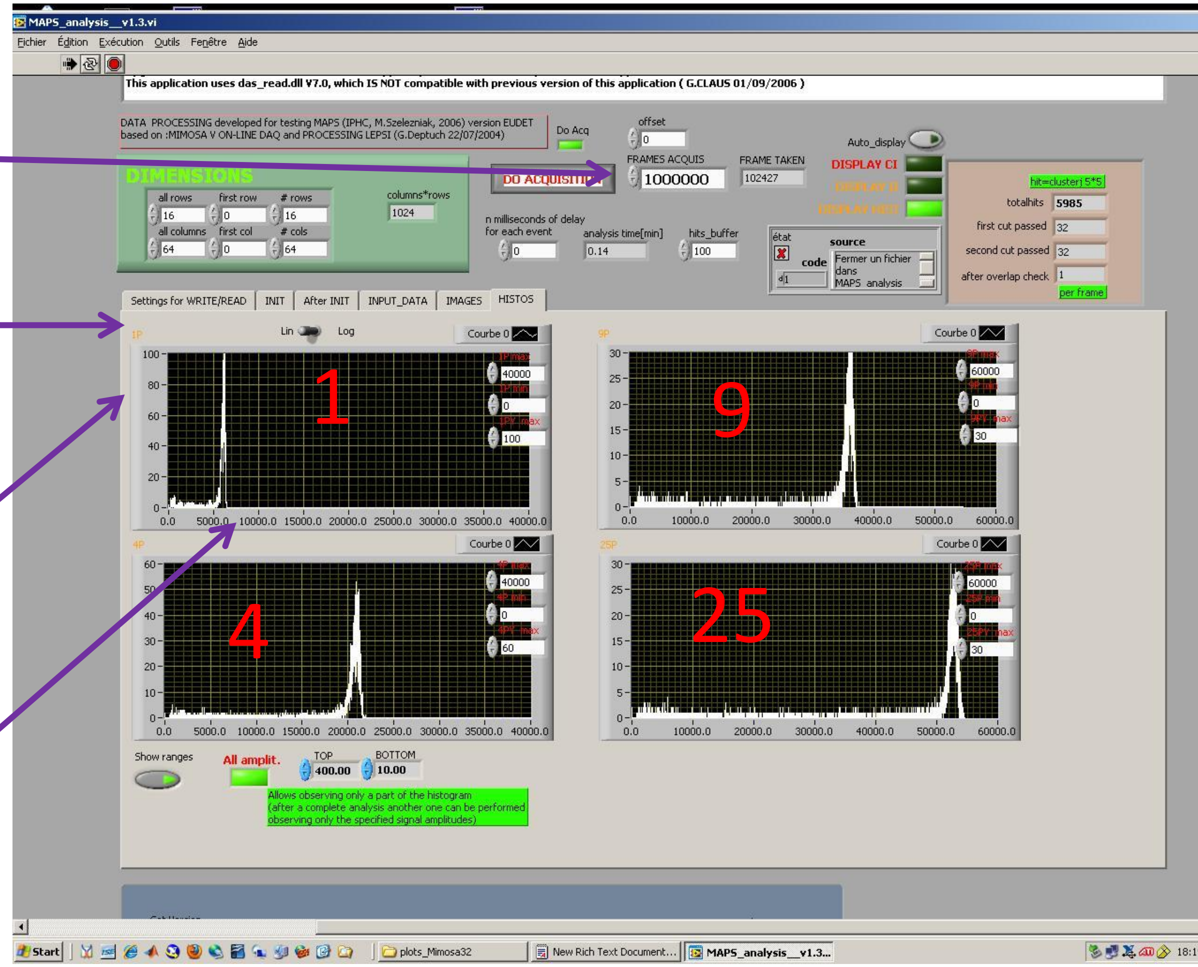
## Laser centered on a pixel

Acquired Frames

Pixel in the cluster

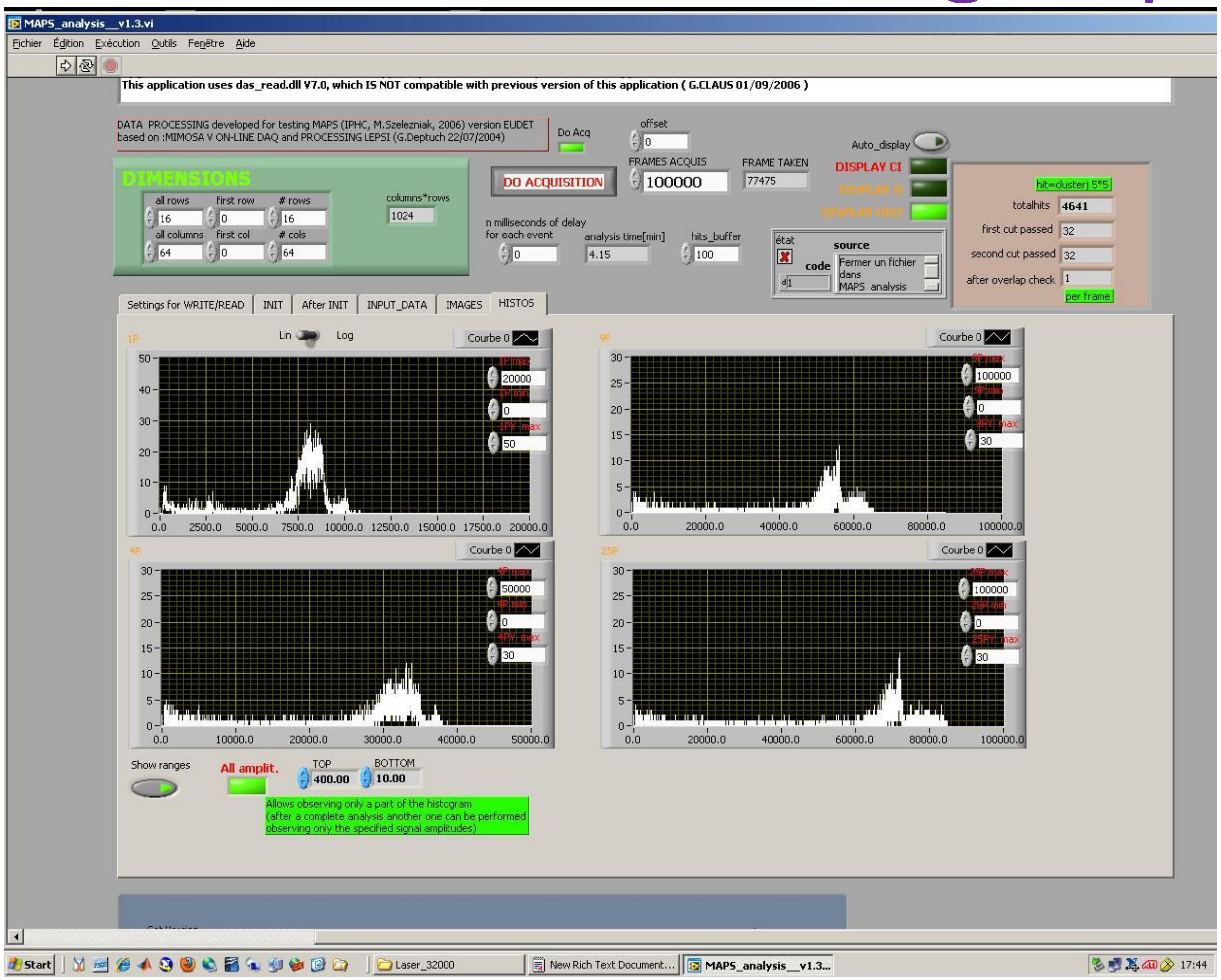
ADC counts (y axis)

Number of entries (x axis)




Measurement done with the PICSEL group in the IPHC (Strasbourg) on a MIMOSA 32 test chip (February 2013)

# Studies to do with laser and chip analog chip




**Laser centered between two pixels** keeping unchanged all the other parameters

With this technique is possible to compare the performances of different collecting diode design

# Plans

Programs for future:

IN BNL:

- With the same setup take data also at the light source  NSLS at the 5-50 keV line.
- Waiting from Strasbourg the for the Mimosa 28 chip and DAQ system with analog readout: with this is possible do charge collection studies with laser.

IN Strasbourg:

- Be involved in the characterization of the final version of the MIMOSA 32 chip

# Simulation/cooling studies

- For the barrel eRHIC silicon detector we are using the STAR PXL ladder design as model.
- Forward/rear part (disks): still to be defined, it will depends on the MIMOSA 32 final design and on the cooling system.
- For the simulation of the impact of the silicon cooling structure in the detector, the plan is to implement a model based on the ALICE upgrade model under development

# Simulation/cooling studies

For the ALICE upgrade the one interesting proposal is a very light cooling system realized with micro-channeling technique on carbon fibers support.